

Lecture 1

Introduction to Circuits and Systems

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Course Aims & Objective

- ❖ Designing Analogue Circuits
 - Real-life operational amplifier, single rail supply
 - Limitation of real op-amps
 - Applications of op-amps
 - SPICE model of op-amps
- ❖ Designing Digital Circuits
 - Field Programmable Gate Arrays
 - Design methods & constraints
 - SystemVerilog Hardware Description Language
- ❖ Systems view of electronic circuits
 - Partitioning between analogue & digital parts in a system
 - Interface between analogue & digital parts

Organization and Schedule

- ❖ Course structure
 - 2-hours **lecture** session on Tuesday @ 14.00 – 16.00
 - 1-hour “**Problem Class**” on Thursday @ 17.00 – 18.00
 - Two 2-hour **laboratory** session on Monday & Tuesday @ 09.00 - 11.00
- ❖ 16 lectures will be supported by:
 - **6 lab experiments** and “open-ended” challenges which will be assessed through two individual Lab Oral sessions
 - **6 problem sheets** to help apply what you have learned to answer questions
- ❖ Assessment:
 - **2-hour written paper** in Summer Term (60%)
 - Mid-term **Lab Oral** (15%)
 - End of Term **Lab Oral** (25%)
- ❖ Please consult the “**EE2 Circuits and Systems Module Description and Planning**” document

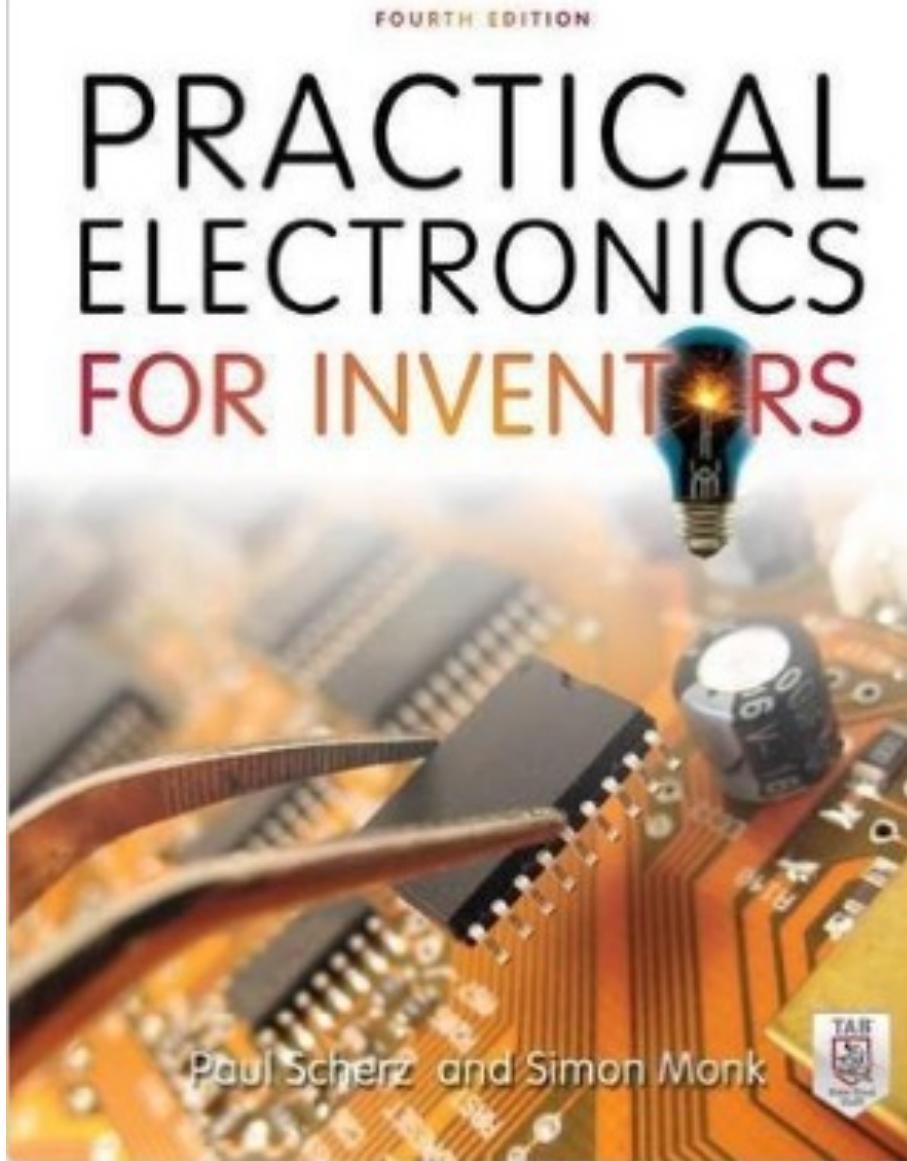
Related Courses

❖ Follow on from these Year 1 modules

- ELEC40002 Analysis and Design of Circuits
- ELEC40003 Digital Electronics & Computer Architecture
- ELEC40004 Programming for Engineers
- ELEC40006 Electronics design project 1

❖ Relevant to these Year 3 and 4 modules

- EE3.01 Analogue Integrated Circuits and Systems
- EE3.02 Instrumentation
- EE3.05 Digital System Design
- EE3.21 Biomedical Electronics
- EE3.24 Embedded Systems
- EE4.16 Analogue Signal Processing
- EE4.17 High Performance Analogue Electronics
- EE4.20 Full-Custom Integrated Circuit Design
- EE4.71 Hardware and Software Verification



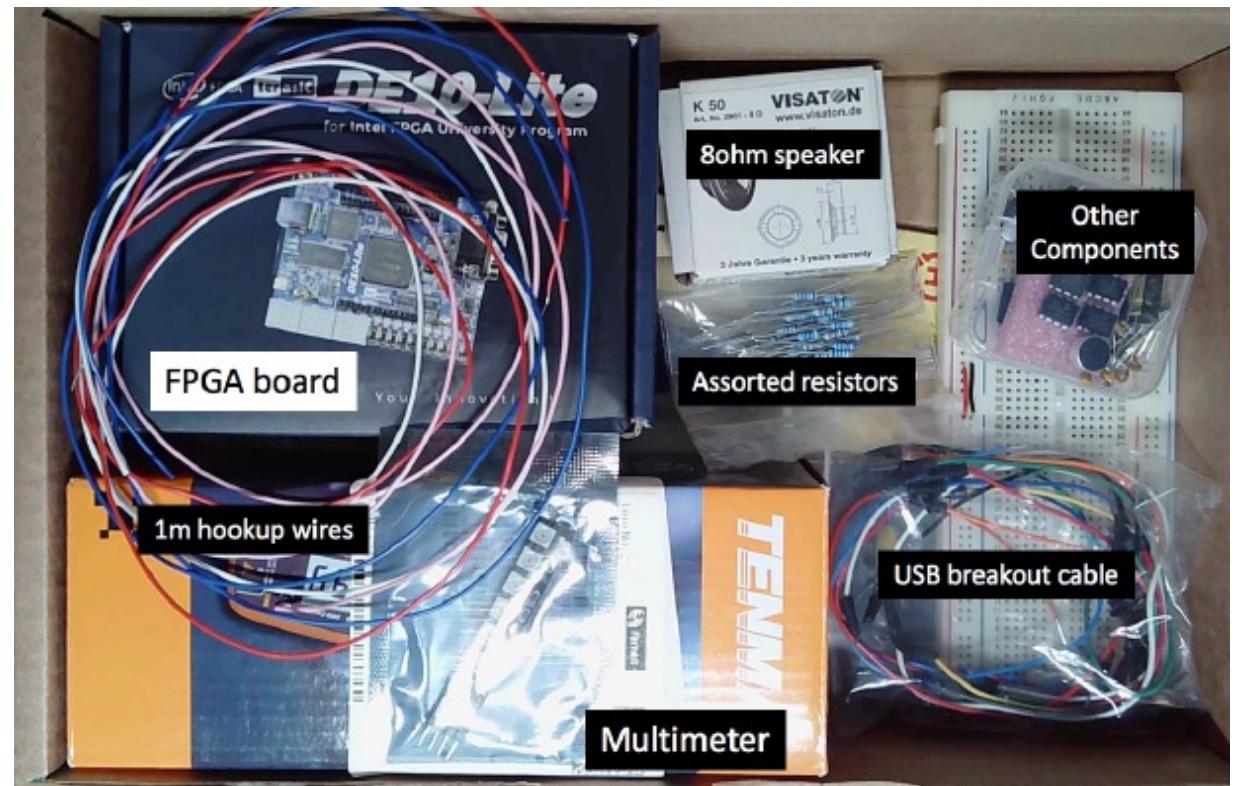
- ❖ Recommended book:
Practical Electronics for Inventors,
Paul Scherz & Simon Monk
- ❖ Useful for analogue part in particular
- ❖ Very useful reference for the future when you want to build electronic circuits
- ❖ Over 1000 pages for under £30 – a bargain!



Lab-in-a-Box

- ❖ Equipment on loan to you to support this module:
 - DE10-Lite FPGA board with prototype shield
 - Prototyping breadboard
 - Other electronics components to support the Lab Experiments

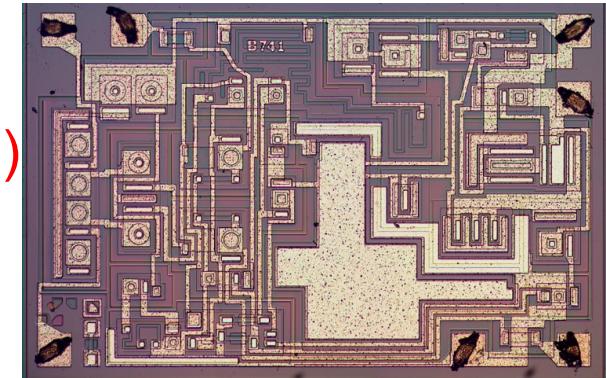
- ❖ **Sustainability** – return the measurement equipment and the FPGA board when finished; reuse other components where possible to minimize waste.
- ❖ Your final Lab Oral marks will not be issued until you have returned the Lab-in-a-Box to the technicians in the Level 1 Lab.



History of Microelectronics

The Transistor (term came from “Transfer Resistor”)

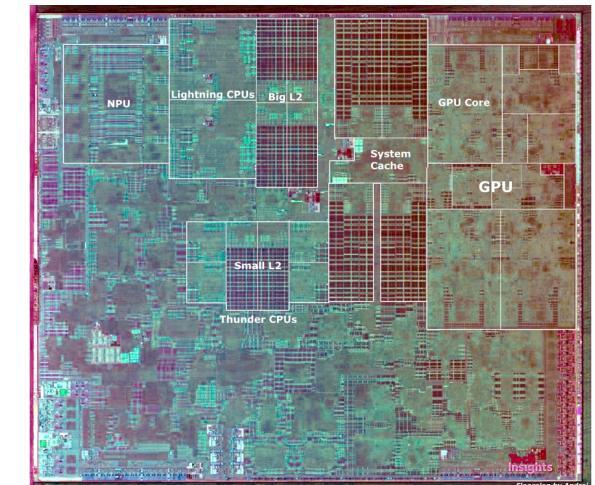
- 1925 – FET concept patented (Lilienfeld, Canada)
- 1942 – Effect observed first in *duodiodes* for radar
- **1947 – First Ge BJT: Bardeen/Brattain/Shockley (Bell)**
- 1954 – First **Silicon BJT**: Teal (TI)
- 1960 – First **MOS Transistor**: Kahng/Atalla (Bell)



741 opamp, 1968

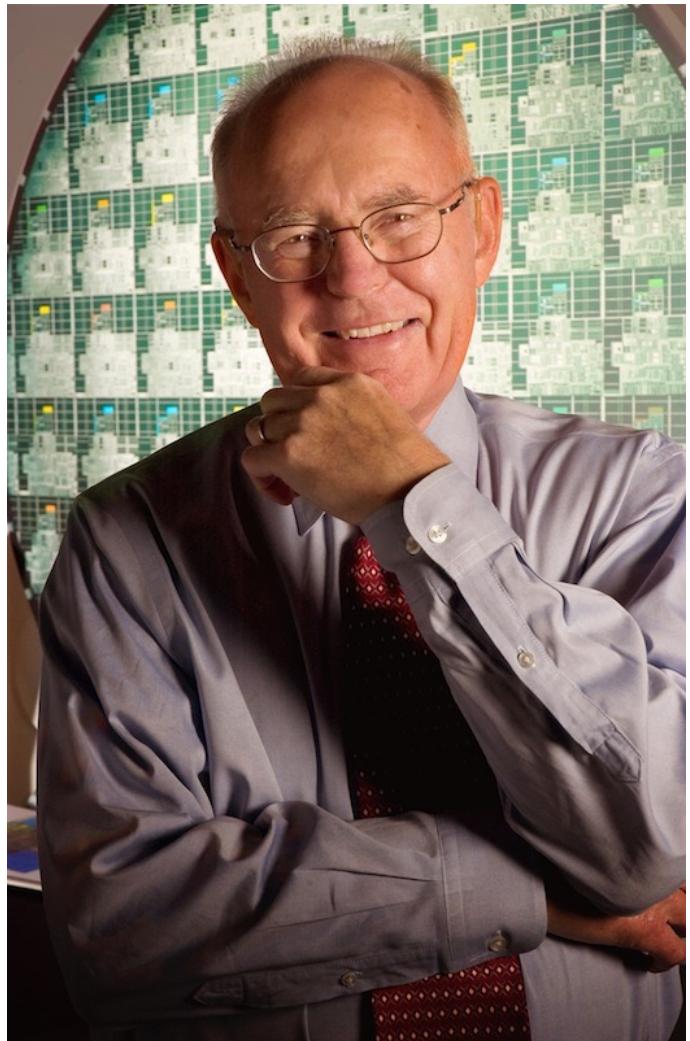
The Integrated Circuit (IC)

- 1952 – IC concept published by Dummer (UK MoD)
- 1958 – **First IC**: Dilby (TI) and Noyce (Fairchild/Intel)
- 1960 – **MSI** (100s of devices integrated per chip)
- **1968 - 20 transistors: 741 opamp**
- 1970 – **LSI** (1000s of devices integrated per chip)
- 1989 – 1m+ transistors on single chip: Intel 80486
- 2008 – 1.7b+ transistors on single chip: Intel Itanium
- 2019 – 8.5b+ transistors on single chip: **Apple A13**



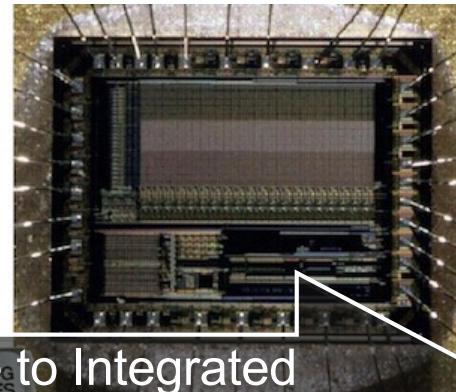
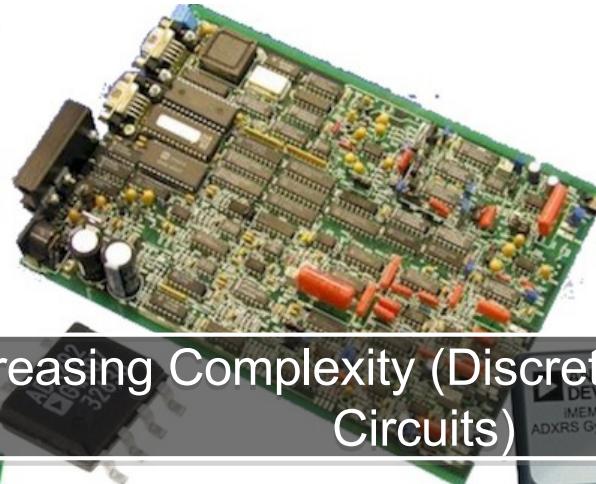
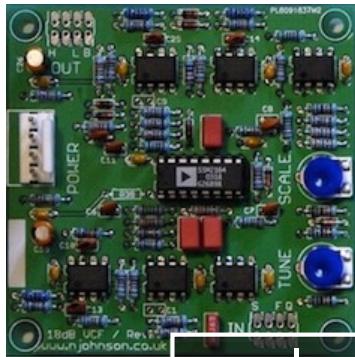
Apple A13, 2019

Moore's Law

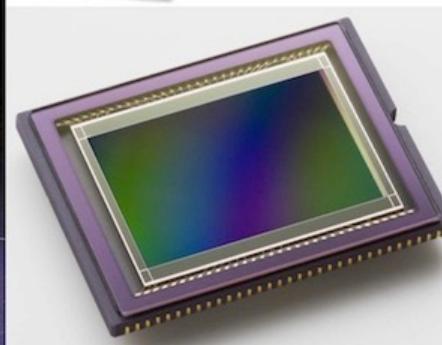
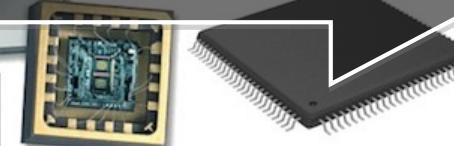
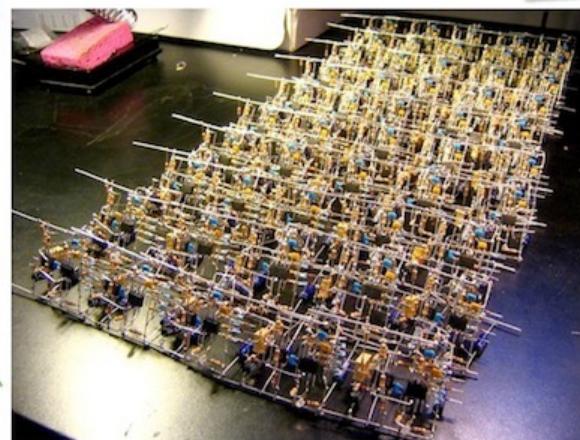


- ❖ **Gordon Moore**, co-founder of Intel, observed in 1965 that number of transistors per square inch in ICs doubled every year.
 - In subsequent years, the pace slowed down a bit, but density has **doubled approximately every 18 months**, and this is the current definition of Moore's Law.
 - This trend has been driving the microelectronics industry – technology target
 - Most experts, including Moore himself, expect Moore's Law to hold for at least another decade.
- ❖ In 2024, **Apple's M4 max chip** has more transistors (90+ billion transistors).

What does electronic system look like?

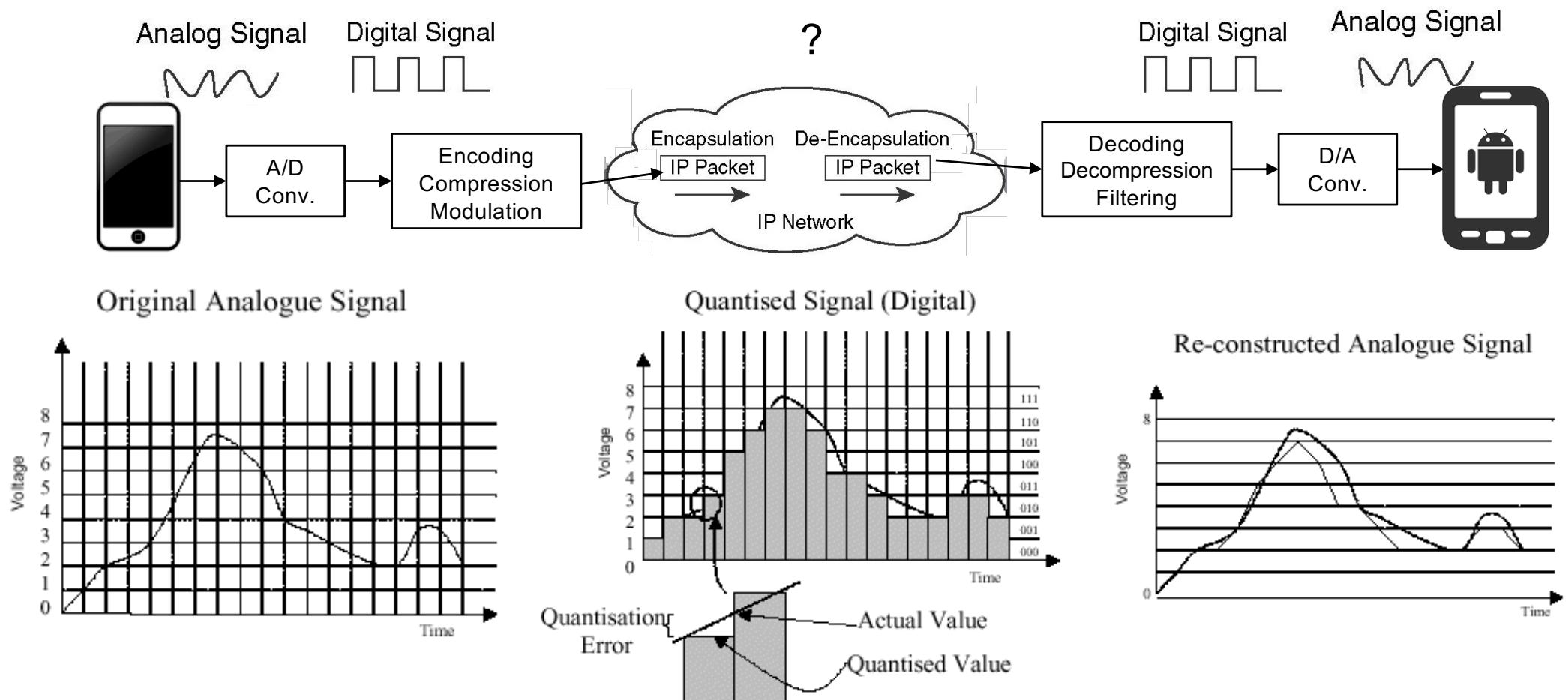


Increasing Complexity (Discrete to Integrated Circuits)



Majalah
Kereta
Online

Analogue vs Digital



- ◆ Most physical phenomena are in the analogue domain.
- ◆ Most modern electronics systems operate in the digital domain.
- ◆ Analogue-to-Digital (A/D) converters, and Digital-to-Analogue (D/A) converters links the two worlds together.

Common Misconceptions (A vs. D)

- ◆ “Analogue electronics is no longer needed – its all done in digital nowadays”
 - All electronics are fundamentally ANALOGUE! Therefore analogue will ALWAYS be needed
- ◆ “Digital is better quality than analogue”
 - No, digital is just more tolerant to interference than analogue
- ◆ “Digital is lower power than analogue”
 - No, in fact in the most demanding applications – analogue is always the more energy efficient
- ◆ “There is no future for an Analogue Design Engineer”
 - There is generally a great shortage of analogue design engineers – therefore there are excellent employment opportunities
 - True – there are more jobs in digital than analogue, as there are more job in software than hardware
 - All digital circuits, at some frequency, are really analogue

Why is analogue design challenging?

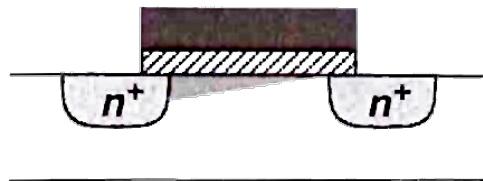
- ❖ Analogue circuits deal with multi-dimensional **tradeoff** of **speed, power, gain, precision, supply, ...**
- ❖ Analogue circuits are much more sensitive to:
 - **Noise, crosstalk**, and other interferers, **second-order device effects**
- ❖ High performance analog circuit design can rarely be automated
 - Typically require **hand-crafted** design and layout
 - Modeling and simulation requires **experience and intuition**
- ❖ Economic forces require the development of analogue circuits in mainstream digital processes (i.e. CMOS technology)
 - Integration of **analogue** and **digital** functions onto a **single substrate**
- ❖ Many levels of abstraction are required

Why is digital design challenging?

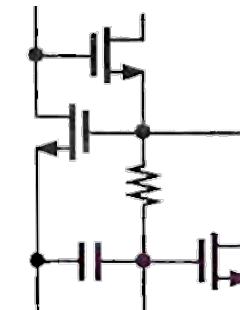
- ❖ Digital circuits deal primarily with **complexity, performance and speed/power trade-off**
- ❖ Complexity leads to many problems:
 - Difficult to **specify**
 - Impossible to breadboard and **prototype**
 - Hard to **verify** design
 - Hard to **test** chip once manufactured
 - **Timing closure** – how to ensure circuit runs reliably at required clock frequency
 - **Partitioning** – how to successfully combine many designer's effort to make a chip
 - Similar issues as in analogue such as **cross-talk, clock distribution and signal integrity**

Level of Abstraction

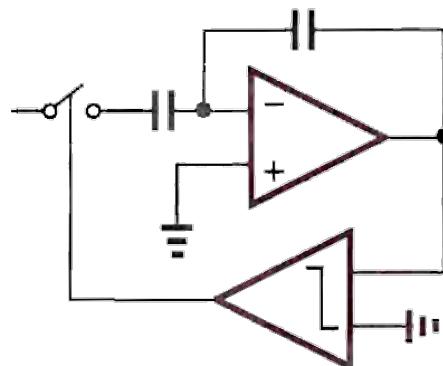
Device-level



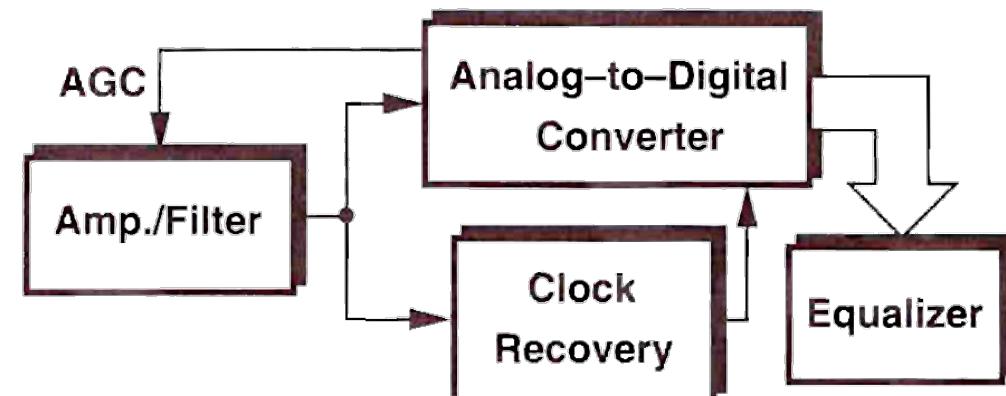
Circuit-level



Architecture-level



System-level



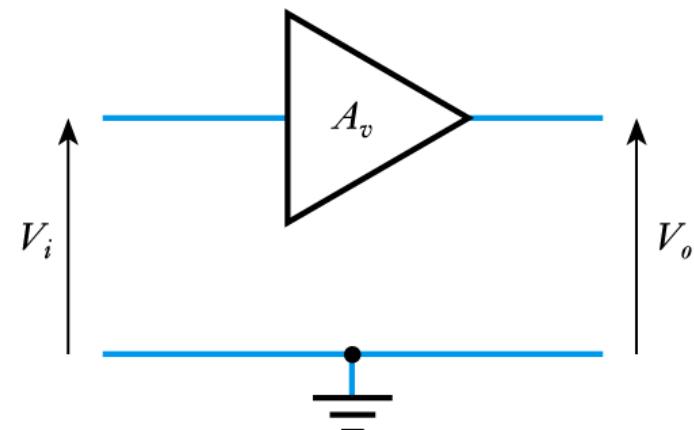
Electronic Amplifiers

- ❖ Revisit electronic amplifiers (covered last year in Holmes/Mitcheson module on analysis of circuits, L9)
 - take power from a power supply
 - amplification described by gain

$$\text{Voltage Gain } (A_v) = \frac{V_o}{V_i} \text{ or } 20 \log_{10} \frac{V_o}{V_i} \text{ dB}$$

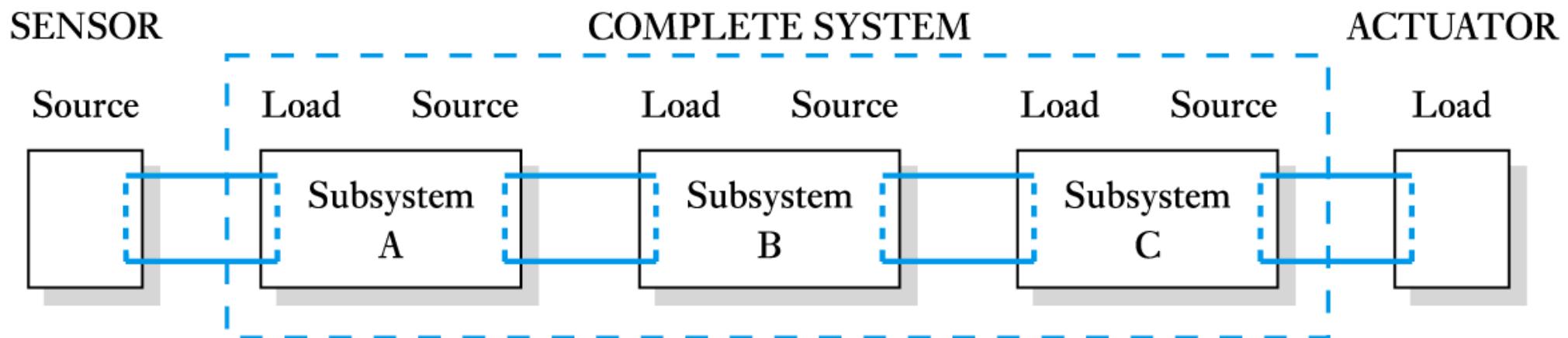
$$\text{Current Gain } (A_i) = \frac{I_o}{I_i} \text{ or } 20 \log_{10} \frac{I_o}{I_i} \text{ dB}$$

$$\text{Power Gain } (A_p) = \frac{P_o}{P_i} \text{ or } 10 \log_{10} \frac{P_o}{P_i} \text{ dB}$$



Sources and Loads

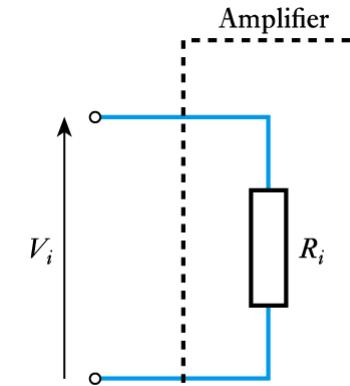
- ❖ An *ideal* voltage amplifier would produce an output determined only by the input voltage and its gain.
 - irrespective of the nature of the source and the load
 - in real amplifiers this is not the case
 - the output voltage is affected by **loading**



Modelling Sources and Loads

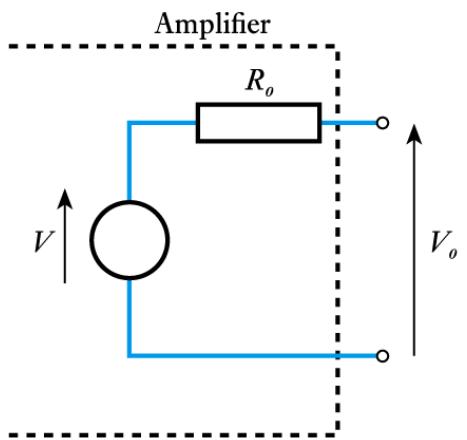
❖ Modelling the input of an amplifier

- the input can often be adequately modelled by a simple resistor
- the **input resistance**



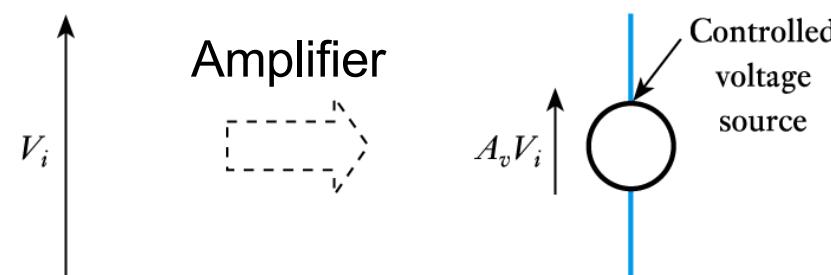
❖ Modelling the output of an amplifier

- Similarly, the output of an amplifier can be modelled by an ideal voltage source and an output resistance.
- This is an example of a **Thévenin equivalent circuit**



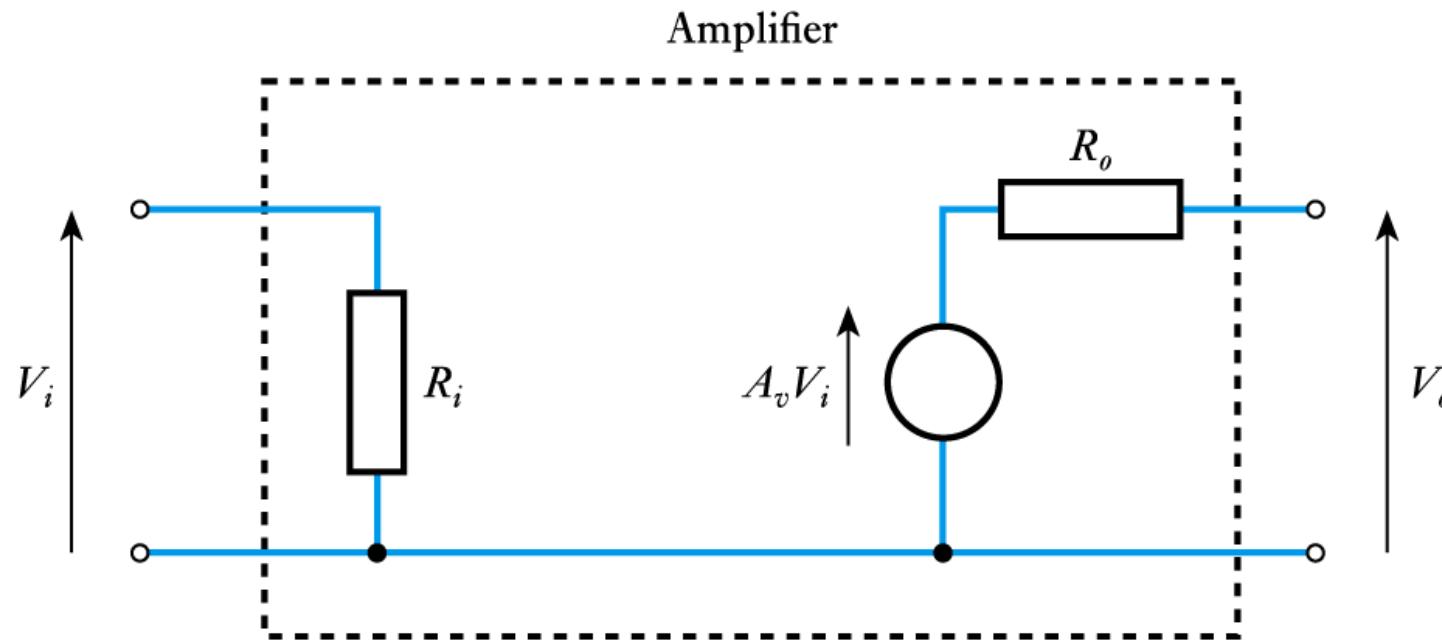
❖ Modelling the gain of an amplifier

- can be modelled by a controlled voltage source
- the voltage produced by the source is determined by the input voltage to the circuit



Equivalent circuit of an amplifier

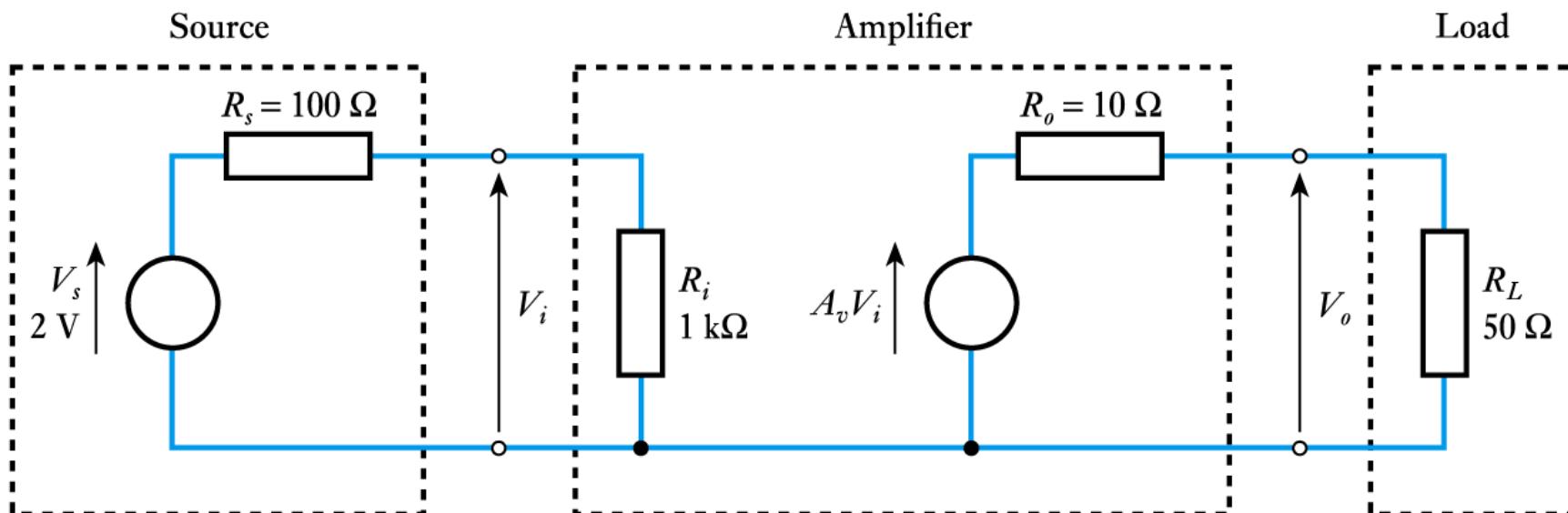
- ❖ We can put together the models for input, output and gain, to form a model of the entire amplifier as shown here



An example (1)

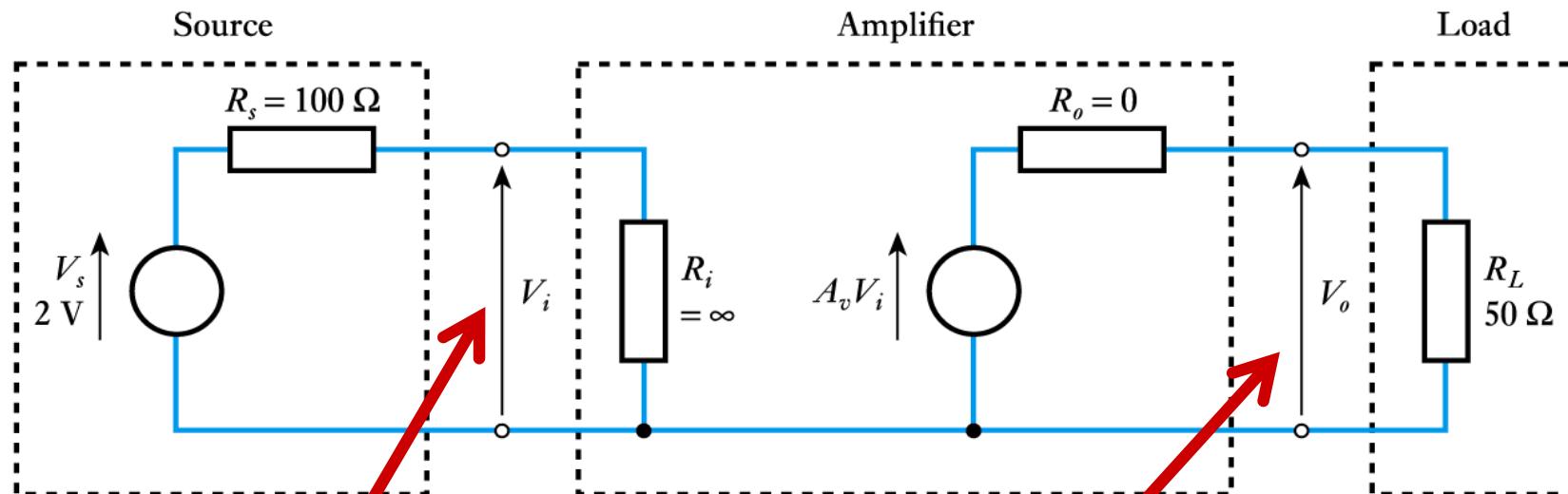
- ❖ An amplifier has a voltage gain of 10, an input resistance of $1\text{ k}\Omega$ and an output resistance of 10Ω .
- ❖ The amplifier is connected to a sensor that produces a voltage of 2 V and has an output resistance of 100Ω , and to a load of 50Ω .
- ❖ What will be the output voltage of the amplifier (that is, the voltage across the load resistance)?

- ❖ We start by constructing an equivalent circuit of the amplifier, the source and the load:



An ideal voltage amplifier

- ❖ An **ideal voltage amplifier** would not suffer from loading
 - it would have $R_i = \infty$ and $R_o = 0$



- ❖ If $R_i = \infty$, then

$$\frac{R_i}{R_s + R_i} \approx \frac{R_i}{R_i} = 1$$

- ❖ and,

$$V_i = \frac{R_i}{R_s + R_i} V_s \approx V_s = 2 \text{ V}$$

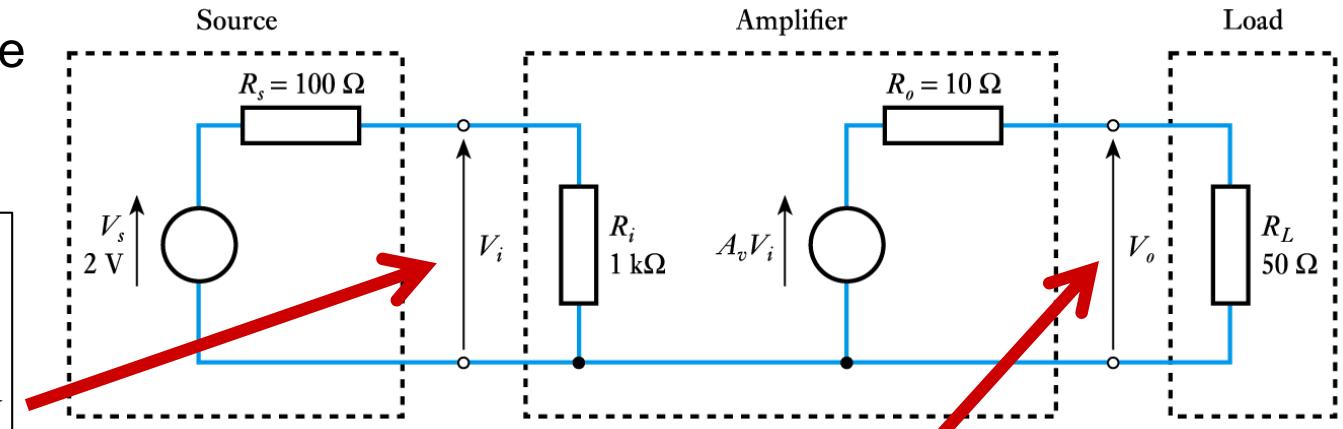
$$\begin{aligned} V_o &= A_v V_i \frac{R_L}{R_o + R_L} \\ &= 10 V_i \frac{50 \Omega}{0 \Omega + 50 \Omega} \\ &= 10 \times 2 \frac{50 \Omega}{50 \Omega} = 20 \text{ V} \end{aligned}$$

An example (2)

- From this we calculate the output voltage:

$$V_i = \frac{R_i}{R_s + R_i} V_s$$

$$= \frac{1 \text{ k}\Omega}{100 \text{ }\Omega + 1 \text{ k}\Omega} \times 2 \text{ V} = 1.82 \text{ V}$$



- Although the amplifier has a gain of 10 when it is NOT connected to anything, when used in the system, the actual gain is:

$$\text{Voltage Gain } (A_v) = \frac{V_o}{V_i} = \frac{15.2}{1.82} = 8.35$$

$$V_o = A_v V_i \frac{R_L}{R_o + R_L}$$

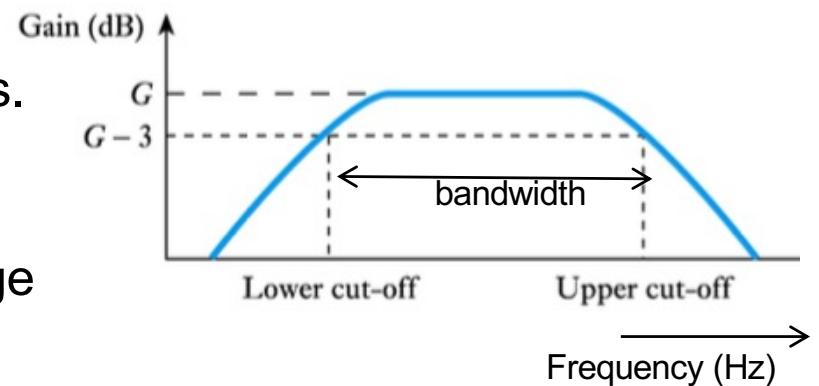
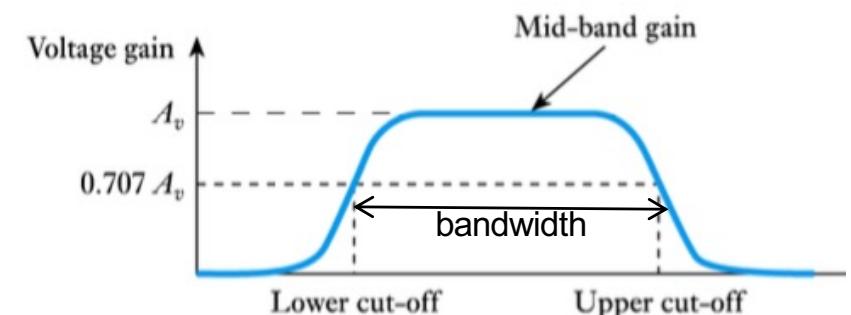
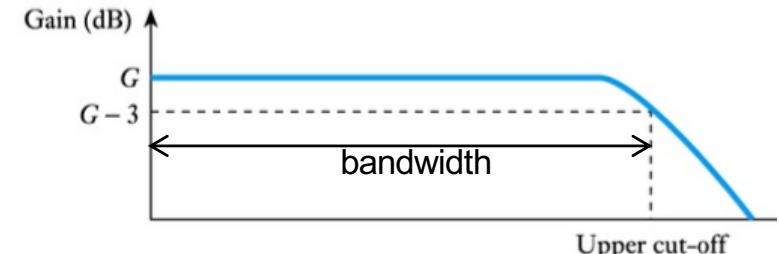
$$= 10 V_i \frac{50 \Omega}{10 \Omega + 50 \Omega}$$

$$= 10 \times 1.82 \frac{50 \Omega}{10 \Omega + 50 \Omega} = 15.2 \text{ V}$$

- The reduction of the voltage gain is due to **loading effects**.
- The original gain of the amplifier in isolation was 10. It is the **unloaded** gain.

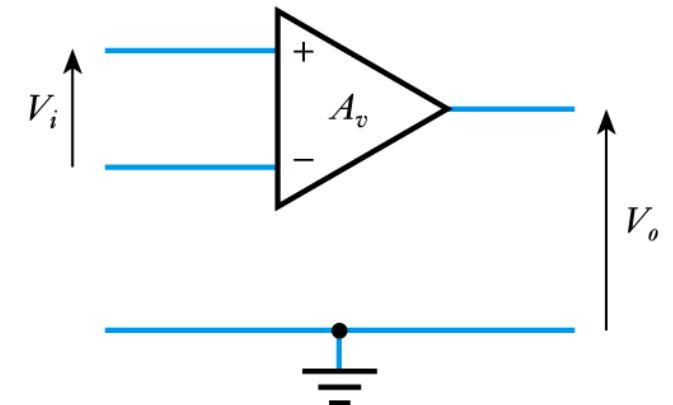
Frequency response and bandwidth of Amplifier

- ❖ All real amplifiers have limits to the range of frequencies over which they can be used.
- ❖ The gain of a circuit in its normal operating range is termed its mid-band gain.
- ❖ The gain of all amplifiers falls at high frequencies.
 - Characteristic defined by the **half-power point**.
 - Gain falls to $1/\sqrt{2} = 0.707$ (-3dB) times the mid-band gain.
 - This occurs at the **cut-off (or corner) frequency**.
- ❖ In some amplifiers gain also falls at low frequencies.
 - These are **AC coupled amplifiers**
- ❖ The bandwidth of the amplifier is the frequency range up to the -3dB point (or cut-off frequencies)

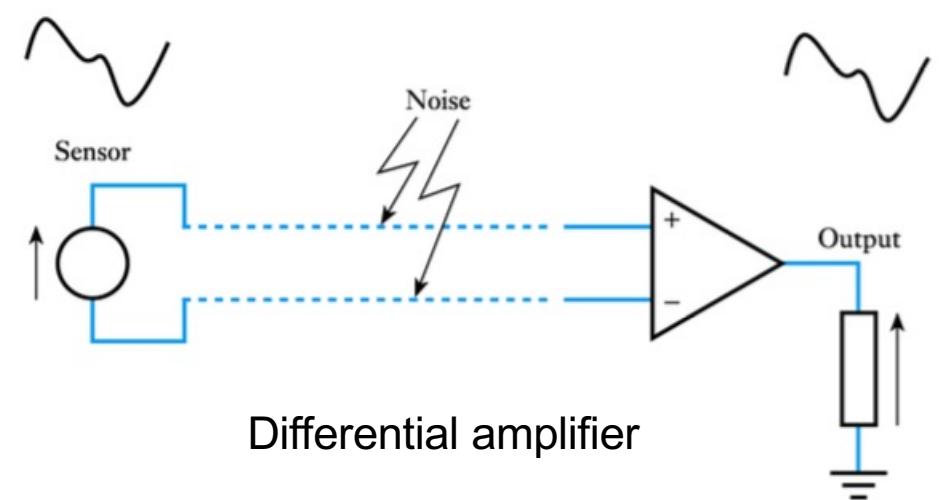
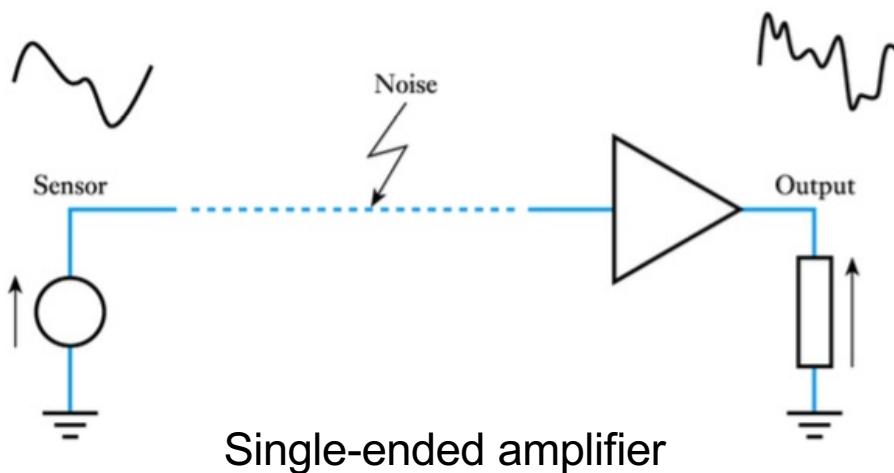


Differential amplifiers

- ❖ Differential amplifiers have two inputs and amplify the voltage difference between them.
 - **non-inverting input** (labelled +) and **inverting input** (labelled -)

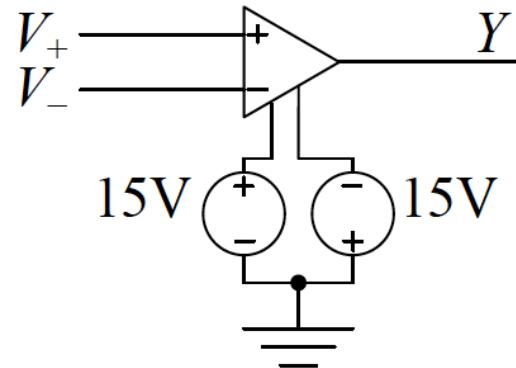


- ❖ An example of the use of a differential amplifier:

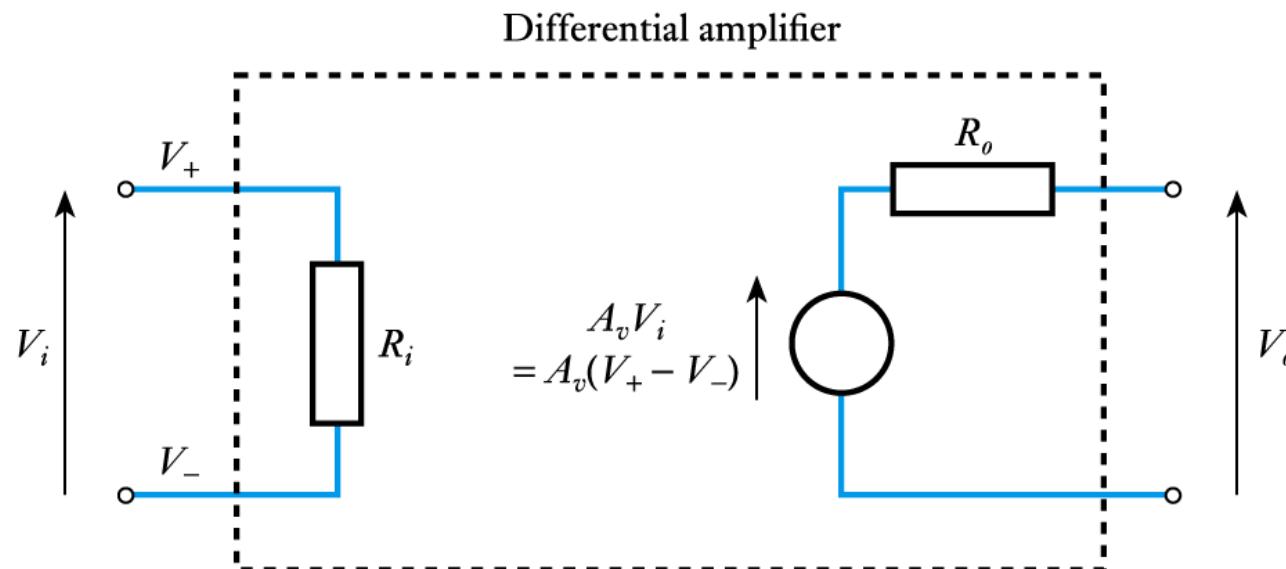


Equivalent circuit of a differential amplifier

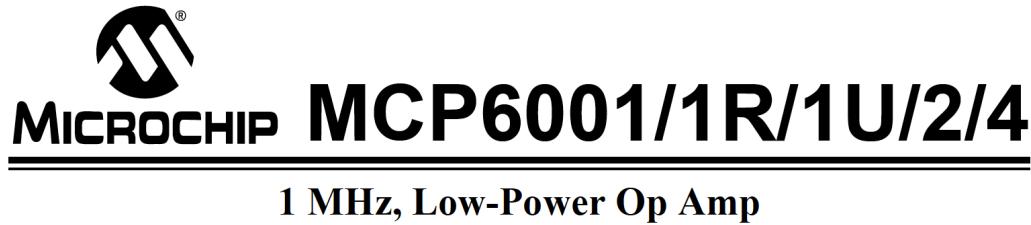
- ❖ Operational Amplifier is a type of differential amplifier (from last year L9S4):



- ❖ The equivalent circuit of such a differential amplifier is:



Real-life Op Amp



Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typical). It also maintains 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100 μ A (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of $V_{DD} + 300$ mV to $V_{SS} - 300$ mV. This family of op amps is designed with Microchip's advanced CMOS process.

- ❖ Limited to 1MHz signal frequency (GBP) (not infinite gain at all frequencies)
- ❖ Stable under high capacitance load (linked to phase margin)
- ❖ **Single power supply operation**
- ❖ **Rail-to-rail input/output swing**
- ❖ Low supply current when idle
- ❖ Near rail-to-rail common mode input voltage